長庚大學 113 學年度第一學期 資訊工程學系博士班資格考 計算機架構 考題

1. A processor's performance can be improved by exploiting more instruction level parallelism.
   (a) The dependency between instructions will reduce the instruction level parallelism. What types of dependencies can exist among instructions?
   (b) How can these dependencies be resolved to minimize their impact on instruction parallelism?

   (15/15 points)

2. There are three data placement policies in cache design: direct mapping, set - associative mapping, and fully associative mapping.
   (a) What are the differences between these policies in terms of cache structure?
   (b) How can these policies affect cache performance?

   (15/15 points)

3. Virtual memory is a memory management mechanism. Answer the following questions regarding virtual memory.
   (a) Explain how a page table is used to translate a virtual address into a physical address.
   (b) Explain how a Translation Lookaside Buffer (TLB) is used to accelerate address translation in virtual memory.

   (15/15 points)

4. Amdahl's Law is a principle that helps to understand the potential performance improvements in a system when only a portion of the system is improved. It is often used in the context of parallel computing to predict the theoretical maximum speedup of a program as a result of enhancing a specific part of it.
   Amdahl's Law can be expressed mathematically as:

$$S = \frac{1}{(1 - P) + P/N}$$

   Where:

   S is the overall speedup of the system.

   P is the proportion of the program that can be improved.

   N is the factor by which that portion can be improved.

   If a program is 75% parallelizable, can we achieve an overall speedup of 2.7 by using a 5-core processor to execute it? Explain your answer using Amdahl's Law.

   (10 points)