長庚大學 114 學年度第一學期 資訊工程學系博士班資格考 計算機架構 考題

1. (20 points) Pipelining is a common technique used in modern processor architecture.
   (a) List two advantages of using pipelining in a processor. (5%)
   (b) Explain how pipelining can improve the throughput of instruction execution. (5%)
   (c) In an ideal pipeline with k stages, the maximum possible speedup is expected to be k. Explain why, in practice, the speedup of pipelining cannot usually reach k. (5%)
   (d) List examples and briefly describe two major factors that cause this performance gap. (5%)

2. (20 points) Cache memory plays an important role in bridging the speed gap between CPU and main memory.
   (a) Explain why cache memory can significantly improve the average memory access time. (5%)
   (b) Briefly describe the difference between write-through and write-back cache policies. (5%)
   (c) What is the main trade-off between a larger cache size and cache access speed? (5%)
   (d) The average memory access time can be determined by three cache variables: hit time, miss rate and miss penalty. In a three-level cache structure, list an equation to explain how these variables at each level will affect the average memory access time. (5%)

3. (20 points) Branch prediction is an important way to reduce the control flow hazards in a processor pipeline.
   (a) Use a code sequence example to explain why and how the branch prediction can improve pipeline throughput. (10%)
   (b) Assume no branch prediction is used, each branch incurs an average 5-cycle delay for a specific processor. Now suppose this processor has a branch prediction design, and the prediction accuracy is 90%, each misprediction incurring a 5-cycle penalty (stall). If a program has 20% branch instructions, how much of the speedup can be obtained with the branch prediction vs. without the branch prediction? Assume the ideal cycle per instruction is one (CPI=1). (10%)

4. (20 points) The processor performance can be improved by exploiting more instruction level parallelism (ILP). The ILP can be exploiting by applying the static instruction scheduling algorithm and the dynamic instruction scheduling algorithm.
   (a) Compare the differences between these two algorithms. (10%)
   (b) In most of cases, the dynamic instruction scheduling algorithm can reduce more pipeline stalls than the static instruction scheduling algorithm. Why? (10%)

5. (20 points) Answer "True" or "False" for the following statements. Explain **why**.
   (a) A processor with a higher clock rate always has higher performance. (5%)
   (b) A pipeline with more stages always has higher performance than a pipeline with less pipeline stages. (5%)
   (c) A 4-core processor always has higher performance than a 2-core processor. (5%)
   (d) A large-size cache always has higher performance than a small-size cache. (5%)